United Electronic Industries

The High-Performance Alternative

DNx-AI-218/228-300

—

User Manual

8-Channel, 24-bit, Simultaneously Sampling, Differential Analog Input Board series with Per-Channel Isolation for the PowerDNA Cube and PowerDNR RACKtangle

August 2019

PN Man-DNx-AI-218/228-300

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Chapter 1 Introduction

This document outlines the feature set and use of the DNx-AI-218 and -228-300. The AI-218/228-300 are 8-channel analog input modules for the PowerDNA I/O Cube (DNA-AI-218/228-300) and the DNR-1G HalfRACK and RACKtangle chassis (DNR-AI-218/228-300). The following products are described in this manual:

- DNx-AI-218: 8-channel ± 10V analog input board
- DNx-AI-228-300: 8-channel ±300V analog input board

The boards are similar, except for their model numbers and voltage ranges.

For a board without channel-to-channel isolation but more channels and with cold-junction compensation, also see the DNA/DNR-AI-217 analog input board.

1.1 Organization of Manual

This User Manual is organized as follows:

- **Introduction**
  This chapter provides an overview of DNx-AI-218/228-300 Analog Input series board features, device architecture, connectivity, and logic.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and interpret results with the Framework API.
- **Programming with the Low-Level API**
  This chapter is an overview of low-level API commands for configuring and using the AI-218/228-300 series board.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-AI-218/228-300 series board.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Bold typeface will also represent field or button names, as in “Click **Scan Network**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbatim into the source code, initialization, or other file.

Before you begin:

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

No HOT SWAP

Always turn POWER OFF before performing maintenance on a UEI system. Failure to observe this warning may result in damage to the equipment and possible injury to personnel.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

1.2 The AI-218/228-300 Interface Board

The DNx-AI-218 and AI-228-300 are 8-channel fully isolated, simultaneously sampling A/D boards compatible with UEI's popular Cube and RACKtangle chassis respectively. The DNA/DNR versions are electronically identical. They feature 24-bit resolution and 7 software-selectable input ranges. Each channel also includes an isolated logic-level DIO bit.

An A/D per channel configuration allows channels to be sampled simultaneously at rates up to 120 kS/s each (480 kS/s max aggregate entire board). The A/D per channel configuration virtually eliminates input cross talk and channel settling time issues even when connected to high impedance signal sources. Each channel is electrically isolated from all other channels as well as from the Cube or RACKtangle chassis, and use dedicated components for each channel.

All connections to the board are through a female DB37 connector. OEMs will find it easy to find mating connectors for custom cables, while end-users may take advantage of UEI's popular DNA-STP-37 screw terminal panel via the DNA-CBL-37 or DNA-CBL-37S series cables.

Software included provides a comprehensive yet easy to use API that supports all popular Windows programming languages as well as supporting programmers using Linux and most real-time operating systems including QNX, RTX, Real-time Linux, VXworks and more. Finally, the UEIDAQ Framework supplies complete support for those creating applications in data acquisition software packages such as LabVIEW, MATLAB/Simulink or any application which supports ActiveX or OPC servers.

1.3 Features

The AI-218/228-300 layer has the following features:

- 8 differential analog input channels
- Simultaneous sampling (one A/D converter per channel)
- Maximum sampling rate 120 kHz per channel (480 kHz max per board)
- 24-bit resolution
- Open wiring detection
- Over-voltage protection
- Differential voltage input of ±10V for AI-218, ±300V for AI-228-300
- Gains - 1, 2, 4, 8, 16, 32 and 64
- Power consumption 4W max
- Weight of 120 g or 4.24 oz for DNA-AI-218/228-300; 630 g or 22.2 oz with PPC5
- Tested to withstand harsh environments
- 8 bits of digital i/o (one per analog input channel)
- UEI Framework Software API may be used with all popular Windows programming languages and most real time operating systems such as Real-time Linux, RTX, or QNX and graphical applications such as Lab-VIEW, MATLAB and any application supporting ActiveX or OPC

1.4 Specification

The technical specification for the DNx-AI-218 board is listed in **Table 1-1**.

Table 1-1. DNx-AI-218 Technical Specifications

Number of channels:	8 fully differential
ADC resolution / type	24 bits / SAR. (AD7766)
Sampling rate	120 kS/s per channel (max); 480 kS/s max aggregate for entire board
Input bias current	< 2 nA typical
Input offset	<4 µV; G=1, <2µV; G=2, <1 µV; G>2 (@ 25°C) (-40°C to +85°C spec is 2.5 times 25°C offset)
Input INL error	< 0.004 % (40 ppm) max
Input impedance	10 MΩ ±1%
Input range	±10 Volt (gain = 1)
Input resolution	1.19 µV (gain = 1), 18.6 nV (gain = 64)
Gains	1, 2, 4, 8, 16, 32, 64
Common mode rejection	110 dB typical
Chan to Chan crosstalk	< 1 µVrms
Isolation	350 Vrms (channel to channel and channel to chassis)
Digital I/O bits	8 (one per isolated A/D channel)
Digital I/O logic levels	Input: 5/3.3 V levels, Output: 3.3 V levels
Overvoltage protection	-40V to +40V (power on or off)
Power off leakage current	< 10 µA (-40V to + 40V)
Power consumption	4.5 W max
Operating temp. (tested)	-40°C to +85°C
Operating humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500Hz, broadband random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
MTBF	290,000 hours

The specification for the AI-228-300 is listed in **Table 1-2**:

Table 1-2. DNx-AI-228-300 Technical Specifications

Number of channels:	8 fully differential and isolated
ADC resolution / type	24 bits / SAR. (AD7766)
Sampling rate	120 kS/s per channel (max); 480 kS/s max aggregate for entire board
Input bias current	< 2 nA typical
Input offset	<120 µV @ 25°C <300 µV from -40°C to +85°C
Input INL error	< 0.0020% (20 ppm) max
Gain error	< 0.005% (50 ppm) max
Input impedance	4 MΩ (min)
Input range	±300 Volt (gain = 1)
Input resolution	35.8µV (gain = 1)
Gains	1, 2, 4, 8, 16, 32, 64
Common mode rejection	110 dB typical (@ DB-37 connector)
Chan to Chan crosstalk	< 120 µVrms (not including cable coupling)
Digital I/O	1 bit per A/D channel. 3.3 V output, 5/3.3 V input
Isolation	350 Vrms (channel to channel and channel to chassis)
Overvoltage protection	-350 V to +350 V (power on or off)
Power off leakage current	< 150 µA (-300 V to + 300 V)
Power consumption	4.5 W max
Operating temp. (tested)	-40°C to +85°C
Operating humidity	95%, non-condensing
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500Hz, broadband random
Shock *IEC 60068-2-27*	100 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
Altitude	120,000 ft
MTBF	200,000 hours

1.5 Comparison between the AI-218 and AI-228-300

The following table is a side-by-side comparison of specification items for the AI-218 and the AI-228/228-300 analog input layers (also see AI-217 manual):

Table 1-3. AI-218 vs.AI-228-300

Item	AI-218	AI-228-300
No. and Type of Channels	8 differential analog voltage	
Input Range	±10V for AI-218	±300V for AI-228-300
A/D Converters	8 differential SAH SAR ADCs	
Sampling	simultaneous sampling on all channels	
Sample Delivery Rate	120 kS/s per channel, 480 kS/s aggregate per board	
CJC	No dedicated CJC channel	
Available Gains	1, 2, 4, 8, 16, 32, 64	
Impedance	Performs well with either low or high impedance sources	
Resolution	24-bit	
Isolation	350Vrms channel-to-channel and channel-to-chassis. Isolated per-channel ground (not common ground).	

Table 1-3. AI-218 vs.AI-228-300 (Forts.)

Item	AI-218	AI-228-300
Pinout	Same for AI-218 and AI-228-300	
Noise Filtering	Simple low-pass RC filter for anti-aliasing before the ADC. After the ADC there is one FIR filter per channel with coefficients settable in groups of 2 channels.	
Channel List	Specifies the channels that are to be read, but because they are simultaneously sampled, a sequential order concept does not apply. The AI-218/228-300 always returns data with the channels in numerical order regardless of what order they were in the channel list. A channel may only appear once in the channel list.	

1.6 Device Architecture

Figure 1-1 is a block diagram of the architecture of the AI-218/228-300 layer.

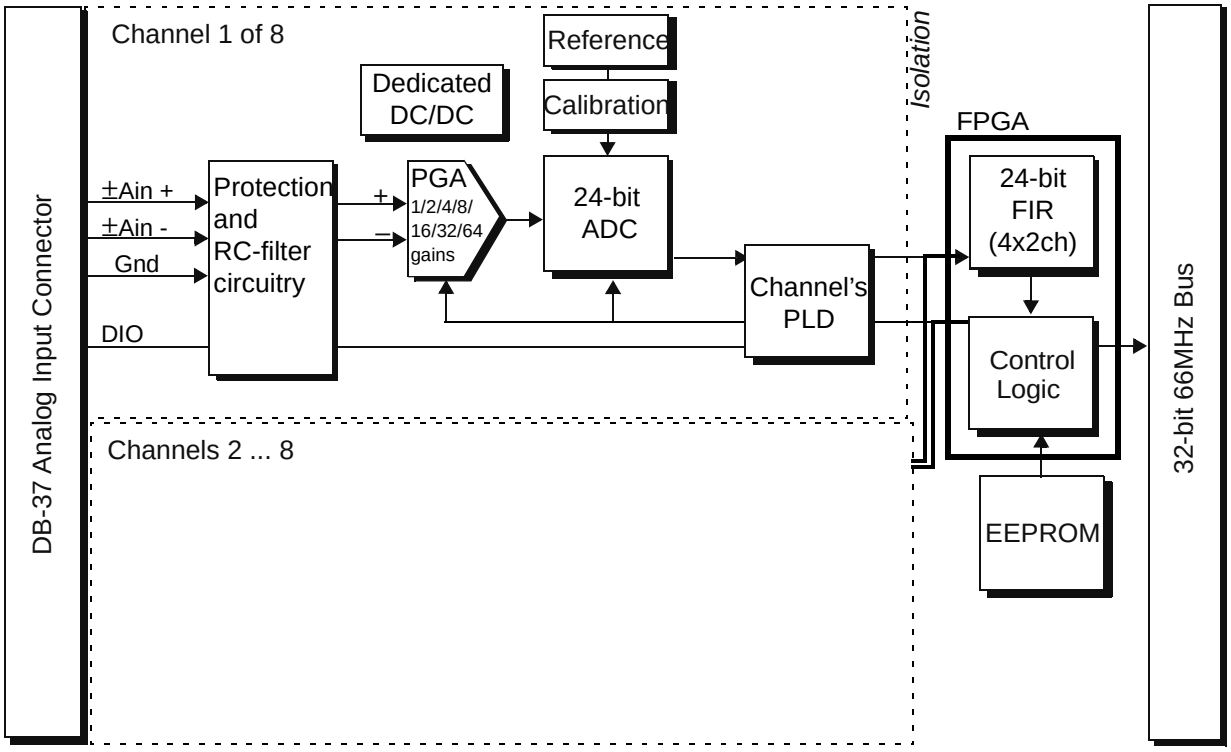


Figure 1-1. Block Diagram of the AI-218/228-300 Board

Each AI-218/228-300 has eight differential input channels designed for high-speed, high-resolution analog voltage signal measurement. Each channel has 24-bit sampling resolution and maximum sampling rate of 120000 samples per second (one sample every 8.3µsec), up to 480000 max samples per second per board. Each channel is individually isolated and uses dedicated components to avoid crosstalk/noise between channels and also ensures that one channel's failure (e.g. due to accidental over-voltage) does not affect other channels or the board.

Each channel's input consists of four pins: a pair of analog input lines that carry the voltage to be sampled, that channel's own ground, and one digital I/O line. The analog input lines (Ain+ and Ain- in **Figure 1-1**) enter through the DB-37 connector pins into a voltage division, protection, and anti-aliasing circuit and are then amplified and sampled, as is described in the next paragraph.

The input lines coming from the connector on the front of the AI-218/228-300 are wired directly into a voltage divider that reduces the input line's voltages down to levels that will be usable by the sampling stage. The difference between these models, in hardware, is the voltage dividers that allow these maximum voltages:

- AI-218: -10V to +10V (shunted; does not use divider)
- AI-228-300: -300V to 300V

The voltage dividers are followed by a protection IC that clips ESD transients to that channel's dedicated DC power supply and by a anti-aliasing RC filter circuit. This protection and filtering circuit is connected to a precision amplifier with seven software-selectable gains to boost the signal by 1, 2, 4, 8, 16, 32, or 64x.

The PGA output is passed into a 24-bit oversampled successive-approximation analog-to-digital converter (described in chapter 1.6.1). Using a single A/D converter for each input channel and per-channel isolation virtually eliminates input crosstalk and channel settling time issues even when connected to high impedance signal sources.

Both the PGA control and the ADC control & data lines are wired to the channel's PLD, which is wired (through an isolation barrier) to the board's main controller; each channel's PLD simplifies access to that channel's PGA, ADC and DIO line.

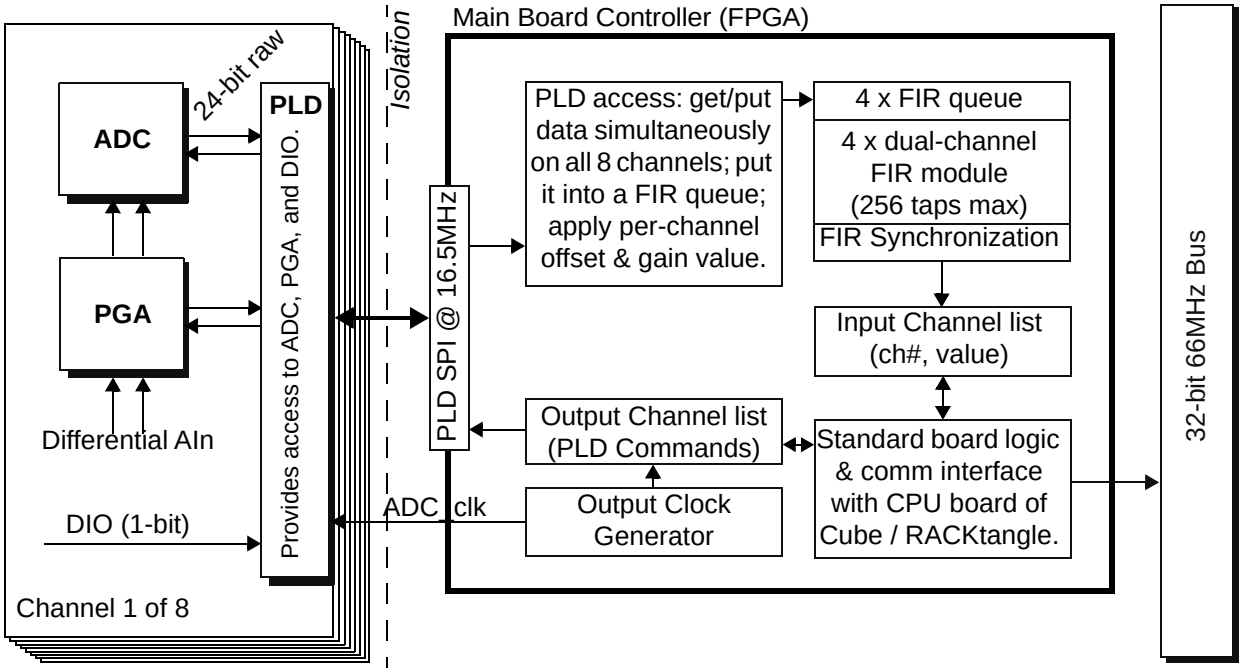


Figure 1-2. Block Diagram of the AI-218/228-300 controllers

In **Figure 1-2** we show how the main controller, in addition to containing the standard logic to provide DNx functionality, also contains AI-218/228-300 specific logic blocks with the role to send commands to all 8 channel PLDs, provide clocking & synchronization, receive & process data from channels, and provide sampled data and configuration access to the Cube & RACKtangle applications.

To set up for a data acquisition sequence of events, the main controller commands the channel's PLD to set the PGA gain and configures ADC clocking, and also configures the internal FIR filter to decimate the (oversampled) ADC values that will be stored in the FIR queue.

To perform data acquisition, the main controller sends a command to sample up to all 8 analog inputs simultaneously, receiving 24-bit raw values from the ADC, to which it will apply the gain/offset adjustments, and push them to the FIR queue. The four two-channel FIR filters process the oversampled ADC values, as described in 1.6.2, and store results in a buffer.

The output buffer is made accessible to standard DNx function calls and is read using software calls in either the UEIDAQ Framework (see Chapter 2) or the low-level API (see Chapter 3).

In addition to each channel's analog inputs *AIn+* and *AIn-*, described above, each channel also has a digital I/O line that can be configured as input or output. You may write to these DIO pins in any configuration, but cannot read from them unless the associated analog input channel is accessed first. The state of the pin is contained in the word of information that is read. The channel's DIO pin is wired through a protection circuit directly to the PLD. Each channel has a GND pin that is also the ground reference for the DIO line; the channel ground references the channel's isolated power supply, and is not connected to the board's common ground nor the chassis's common ground.

1.6.1 Analog to Digital Conversion

The AI-218/228-300 implements ADC converters that utilize oversampled SAR architecture and need a clock source that is 8 times that of the output data rate. The input clock source for the ADCs is kept between 480KHz to 960KHz, meaning that the actual data rate from the ADC is 60000-120000 samples/sec.

To get output data rates less than 60kHz the layer's *FIR module's* decimation unit will only keep 1 in n samples, where n is the decimation factor. The following pseudocode shows how to calculate the master clock frequency and the decimation ratio for the AI-218, which is useful when not using the on-layer clock:

```
// calculate decimation factor and sample rate

decratio = 1;
while (mclkrate <= (480000/8)){  // start at 60000Hz
        mclkrate *= 2;
        decratio *= 2;
}
```

The AI-218/228-300 provides a special clock divider that can use 66MHz as well as fixed 21.12MHz or 25.6MHz clocks to create different frequencies used to run the ADC; the AI-218/228-300[1] incorporates a programmable PLL that allows the generation of the base frequency with 0.1% or better accuracy. Alternatively the UEI DNx-IRIG-650 layer's 100MHz base clock and PLL can also be used to generate a very precise master clock signal of 480-960KHz and route it into the AI-218/228-300 ADCs. The "master" clock shall be constantly running even when conversion results are not used because it has a long FIR filter that should stay settled (see AD7766/AD7767 datasheet for details about the ADC). Thus, samples are always produced, but are not stored in the output buffer until a start command or start trigger is issued.

When multiple boards need to be synchronized, the clock from the master layer can be routed to the SYNC bus and from there back to the clock of slave boards. Keeping all boards synchronized using the 8x ADC clock and hardware trigger should provide fully synchronous operation of multiple layers; however if there are other layers in the system that require synchronization using the scan clock there are two other options that should be considered. One is to take an 8x clock from the SYNC bus, divide it by 8 using the CT-601 layer and then re-distribute it across another SYNC line. However if an extra layer is not an option there is an additional possibility to synchronize the AI-218/228-300 using the scan clock – each individual layer is configured to run ADC at maximum rate of 120kHz and

1. This feature is supported on logic revision 02.10.D3 (2013). UEI Technical Support can provide you with a field programmable update package if your logic is older. Use
PowerDNA Explorer's Hardware Report to show logic versions for your AI-218/228.

scan clock used as a gate that grabs one last scan received from the converters. This way all layers are synchronized within ±1 conversion cycle (8.3µsec).

1.6.2 FIR Filter & Decimation

A unique feature of the AI-218/228-300 is the use of four 2-channel (i.e. 0 to 1, 2 to 3, 4 to 5, 6 to 7) FIR filters implemented on-chip in the *FIR module* logical block. Each channel uses its own storage for the data and each two channels share the same coefficients and decimation ratio. By default, all channels are set to the same coefficients and decimation ratio by the software function call for simplicity, and thus have the same output data rate. Coefficients and decimation ratio are automatically selected by the software calls to an optimum value to match the throughput. The FIR filter can either be disabled or enabled with automatic or user-configured coefficients using software function calls. The *FIR module's* decimation ratio can also be user-configured to 0 (keep all samples) or a decimation factor, *n*, such that 1 in *n* samples are kept and the rest discarded.

This section discusses the configuration of the digital FIR filter found in the *FIR module* logical block. This should not be confused with the FIR filters also found in the AD7766 (as per its datasheet), or the anti-aliasing filter circuit on the front-end of the PGA discussed much earlier.

The *FIR module* implements an integer-based finite-input-response filter with 256 taps. The default filter is configured to suppress harmonics above one half of the ADC output data rate, however, you can generate a set of your own filter coefficients, which you can configure the AI-218/228-300 to use.

The filter operates as per standard digital FIR filter theory:

1. The newest input sample from the ADC is put into the delay line register.
2. Each sample in the delay line is multipled by the corresponding coefficient. Accumulate all multiplied values to provide the result to the output line.
3. Shift the delay line by one sample to make room for the next input sample.

The caveats of using the FIR filter are that rippling may occur in response to sharp edges and there is a group delay of 256/2=128 ADC samples before the output is provided into the output buffer.

1.7 Diagnostics

A standard feature available with the AI-218/228-300 is a diagnostic function called `DqAdv217GetPgaStatus()`. You can call this function at any time to perform a series of diagnostic tests of board operation. Refer the PowerDNA API Reference Manual for a detailed description of how the function works.

1.8 Indicators

A photo of the DNR-AI-218/228-300 unit is illustrated below.

The front panel has two LED indicators:

- RDY: indicates that the layer is receiving power and operational.
- STS: can be set by the user using the low-level framework.

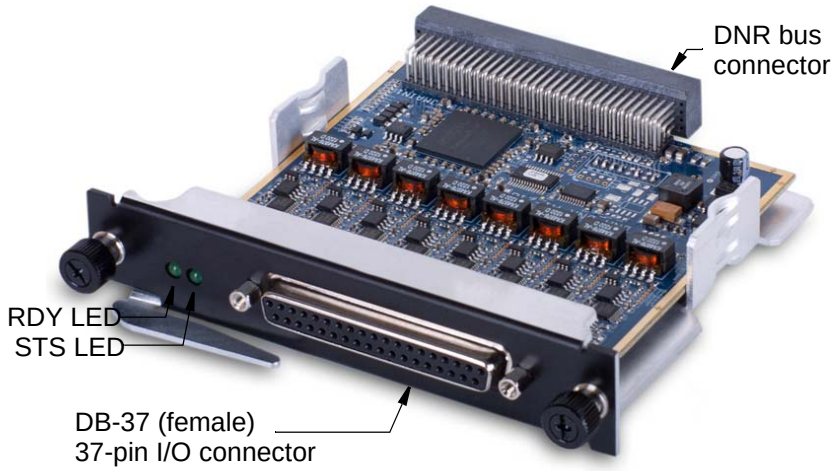


Figure 1-3. The DNR-AI-218/228-300 Analog-Input Layer

1.9 Layer Connectors and Wiring

Figure 1-4 below illustrates the pinout of the AI-218/228-300. The layer uses a B-size 37-pin D-sub connector. The following signals are located at the connector:

- AINx+ and AINx- — input channel, differential mode
- GNDx — analog/digital ground, wired to each channel's power supply
- DIOx — the channel's digital input/output line
- RSVD — reserved for internal use; do not connect to this pin

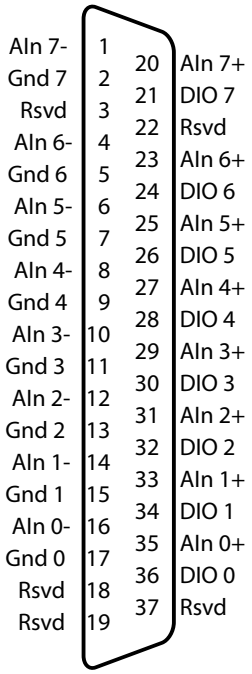


Figure 1-4. Pinout Diagram of the AI-218/228-300 Layer

NOTE: If you are using a accessory panel with the AI-218/228-300, please refer to the Appendix for a description of the panel.

Chapter 2 Programming with the High Level API

This section describes how to control the DNx-AI-218/228-300 using the UeiDaq Framework High Level API.

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.1 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input
CUeiSession aiSession;
```

2.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ai0:3” as a range, or as a list “pdna://192.168.100.2/Dev1/Ai0,1,2,3”.

2.3 Configuring the Input

This section will show you how to configure your input for voltage measurement, thermocouple measurement, or RTD measurement.

2.3.1 Voltage Measurement

The gain applied on each channel is specified by using low and high input limits.

For example, the AI-218 available gains are 1, 2, 4, 8, 16, 32, 64 and the maximum input range is [-10V, +10V (gain = 1)].

To select the gain of 1, you need to specify input limits of [-10V, +10V]:

```
// Configure channels 0,1 to use a gain of 1 in differential mode
aiSession.CreateAIChannel(“pdna://192.168.100.2/Dev0/Ai0,1”,
                          -10.0, 10.0,
                          UeiAIChannelInputModeDifferential);
```

2.4 Configuring the Timing

You can configure the AI-218/228-300 to run in simple mode (point by point) or high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode.

In simple mode, the delay between samples is determined by software on the host computer. In buffered mode, the delay between samples is determined by the AI-218/228-300 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)
aiSession.ConfigureTimingForSimpleIO();
```

2.5 Read Data

Reading data is done using *reader* object(s). There is a reader object to read raw data coming straight from the A/D converter. There is also a reader object to read data already scaled to volts or mV/V.

The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session’s stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan, where the buffer will contain one value per channel
aiReader.ReadSingleScan(data);
```

2.6 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session
aiSession.CleanUp();
```

Chapter 3 Programming with the Low-level API

The PowerDNA cube and PowerDNR RACKtangle and HalfRACK can be programmed using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to access device registers directly.

However, we recommend that, when possible, you use the UeiDaq Framework High-Level API (see **Chapter 2**), because it is easier to use. You should need to use the low-level API only if you are using an operating system other than Windows.

For additional information about low-level programming of the AI-218/228-300, please refer to the PowerDNA API Reference Manual document under:

Start » Programs » UEI » PowerDNA » Documentation

Refer to the PowerDNA API Reference Manual on how to use the following low-level functions of AI-218/228-300, as well as others related to cube operation:

Function	Description
`DqAdv217Read`	Returns continously sampled data from input channel.
`DqAdv217GetPgaStatus`	Returns the PGA status of the AI-218 or AI-228.
`DqAdv217SetCfgLayer`	Set advanced layer configuration parameters for the AI-218/228.
`DqAdv217SetFIR`	Sets the FIR configuration for one or more channels.
`DqAdv217SetPll`	Configures custom sampling rates for DACs.
`DqAdv218ConfigDio`	Sets direction of digital channels to input or output.
`DqAdv218WriteDioOut`	Write to a pre-configured digital output port. Returns old value.

Appendix A

A. Accessories

The following cables and STP boards are available for the AI-218/228-300 layer.

DNA-CBL-37

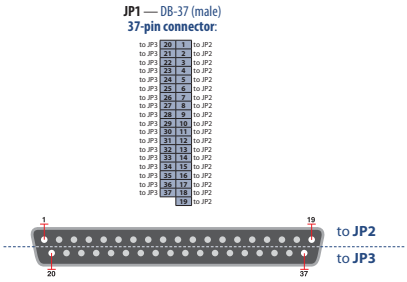
This is a 37-conductor flat ribbon cable with 37-pin male D-sub connectors on both ends. The length is 3ft and the weight is 3.4 ounces or 98 grams.

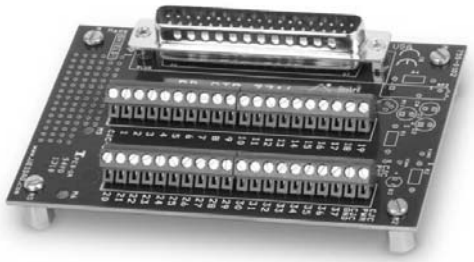
DNA-CBL-37S

This is a 37-conductor round shielded cable with 37-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 3 ft (90 cm) long, weight of 10 ounces or 282 grams; also available in 10ft and 20ft lengths.

DNA-STP-37

The DNA-STP-37 provides easy screw terminal connections for all DNA and DNR series I/O boards which utilize the 37-pin connector scheme. The DNA-STP-37 is connected to the I/O board via either DNA-CBL-37 or DNA-CBL-37S series cables. The dimensions of the STP-37 board are 4.2w x 2.8d x1.0h inch or 10.6 x 7.1 x 7.6 cm (with standoffs). The weight of the STP-37 board is 2.4 ounces or 69 grams.





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